TRANSPARENT ERROR CORRECTING MEMORY

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ABSTRACT

A memory system with transparent error correction circuitry provides full stuck-at fault coverage for both test data patterns and the corresponding error correction code (ECC) values. The memory system includes a semiconductor memory having a memory array, a memory interface and an error detection/correction unit. The memory array is configured to store test data patterns and corresponding error correction code (ECC) values. The memory interface is configured such that the ECC values are not directly accessible. The error detection/correction unit is configured to correct single-bit errors in the test data patterns and corresponding ECC values. A set of test data patterns associated with the semiconductor memory is selected such that any multiple-bit error in a test data pattern and the corresponding ECC value causes the error detection/correction unit to provide an output data pattern having an error, thereby rendering multiple-bit faults 100% detectable.